CLAIMS

1. A semiconductor structure, comprising:

(i) a substrate;

(ii) a charge-trapping structure on said substrate; and

(iii) a gate on said substrate;

wherein said charge-trapping structure comprises:

(a) a first ONO structure on a first portion of said substrate;

(b) a second ONO structure on a second portion of said substrate, wherein said first portion does not completely overlap said second portion;

(c) a gate oxide between said first and second ONO structures; and

said ONO structures comprise a nitride layer between a first oxide layer and a second oxide layer.

2. The device of claim 1, wherein said gate is on said gate oxide and said ONO structures.

3. The device of claim 1, wherein said gate is on only said gate oxide.

4. The device of claim 3, wherein said second oxide layer is thicker than said first oxide layer.

5. A method of forming a semiconductor structure, comprising:

forming a charge-trapping structure on a substrate;

wherein said charge-trapping structure comprises:

(i) a first ONO structure on a first portion of said substrate;

(ii) a second ONO structure on a second portion of said substrate, wherein said first portion does not completely overlap said second portion; and

(iii) a gate oxide between said first and second ONO structures; and

said ONO structures comprise a nitride layer between a first oxide layer and a second oxide layer.

6. The method of claim 5, wherein said forming comprises:

forming an oxide-conductive layer on said substrate, said oxide-conductive layer comprising a first conductive layer on a thick oxide layer;

laying down a bit line mask of photoresist, said bit line mask formed generally in columns at least within a memory portion of said substrate;

removing at least a portion of said oxide-conductive layer wherever said photoresist is not present to form oxide-conductive-layer columns comprising said gate;

implanting bit lines wherever said photoresist is not present and generally in columns;

removing said photoresist;

removing a portion of said remaining thick oxide layer from said oxide-conductive-layer columns to form a recess and said gate oxide;

growing a thin oxide layer over said memory portion of said substrate, the portion of said thin oxide layer in the lower region of said recess forming said first oxide layer and the portion of said thin oxide layer in the upper region of said recess forming said second oxide layer;

depositing a nitride layer over said thin oxide layer to a thickness sufficient to fill said recess; and

removing said nitride layer except in the region of said recess to form said ONO structures.

7. The method of claim 6, further comprising:

forming bit line dielectrics on said bit lines; and

removing said thin oxide layer from the top surface of said oxide-conductive-layer columns.

8. The method of claim 7, further comprising depositing a second conductive layer on said substrate.

9. The method of claim 8, further comprising concurrently etching said first and second conductive layers to form word lines perpendicular to and on said bit line dielectrics and said oxide-conductive-layer columns.

10. A method of forming a semiconductor device, comprising:

making a semiconductor structure by the method of claim 5; and

forming a semiconductor device from said semiconductor structure.

11. A method of making an electronic device, comprising:
making a semiconductor device by the method of claim 10; and
forming an electronic device comprising said semiconductor device.

12. A method of forming a semiconductor device, comprising:
making a semiconductor structure by the method of claim 6; and
forming a semiconductor device from said semiconductor structure.

13. A method of making an electronic device, comprising:
making a semiconductor device by the method of claim 12; and
forming an electronic device comprising said semiconductor device

14. The method of claim 5, wherein said forming comprises:
forming an oxide-conductive layer on said substrate, said oxide-conductive layer comprising a first conductive layer on a thick oxide layer;
laying down a bit line mask of photoresist, said bit line mask formed generally in columns at least within a memory portion of said substrate;
removing at least a portion of said oxide-conductive layer wherever said photoresist is not present to form oxide-conductive layer columns comprising said gate on said gate oxide;
implanting bit lines wherever said photoresist is not present and generally in columns;
removing said photoresist; and
forming an ONO layer within said memory portion of said substrate, said ONO layer comprising said nitride layer between said first oxide layer and said second oxide layer;
removing said ONO layer except from the regions adjacent to said oxide-conductive-layer columns to form said ONO structures.

15. The method of claim 14, further comprising:
forming bit line dielectrics on said bit lines and said ONO structures; and
removing said thin oxide layer from the top surface of said oxide-conductive-layer columns.

16. The method of claim 15, further comprising depositing a second conductive layer on said substrate.

17. The method of claim 16, further comprising concurrently etching said first and second conductive layers to form word lines perpendicular to and on said bit line dielectrics and said oxide-conductive-layer columns.

18. A method of forming a semiconductor device, comprising:
making an semiconductor structure by the method of claim 14; and
forming a semiconductor device from said semiconductor structure.

19. A method of making an electronic device, comprising:
making a semiconductor device by the method of claim 14; and
forming an electronic device comprising said semiconductor device.

20. The method of claim 5, wherein said forming comprises:
forming an oxide-conductive layer on said substrate, said oxide-conductive layer comprising a first conductive layer on a thick oxide layer;
within a memory portion of said substrate, removing at least a portion of said oxide-conductive layer to form oxide-conductive-layer columns comprising said gate;
implanting bit lines between said oxide-conductive-layer columns;
removing a portion of said remaining thick oxide layer from said oxide-conductive-layer columns to form a recess and said gate oxide;
growing a thin oxide layer over said memory portion of said substrate, wherein the portion of said thin oxide layer in the lower region of said recess forms said first oxide layer and the portion of said thin oxide layer in the upper region of said recess forms said second oxide layer;
depositing a nitride layer over said thin oxide layer to a thickness sufficient to fill said recess; and
removing said nitride layer except in the region of said recess to form said ONO structures.

21. The method of claim 20, further comprising:
forming bit line dielectrics on said bit lines; and

removing said thin oxide layer from the top surface of said oxide-conductive-layer columns.

22. The method of claim 21, further comprising depositing a second conductive layer on said substrate.

23. The method of claim 22, further comprising concurrently etching said first and second conductive layers to form word lines perpendicular to and on said bit line dielectrics and said oxide-conductive-layer columns.

24. The method of claim 5, wherein said forming comprises:

forming an oxide-conductive layer on said substrate, said oxide-conductive layer comprising a first conductive layer on a thick oxide layer;

within a memory portion of said substrate, removing at least a portion of said oxide-conductive layer to form oxide-conductive layer columns comprising said gate on said gate oxide;

implanting bit lines between said oxide-conductive layer columns;

forming an ONO layer within said memory portion of said substrate, said ONO layer comprising said nitride layer between said first oxide layer and said second oxide layer; and

removing said ONO layer except from the regions adjacent to said oxide-conductive-layer columns to form said ONO structures.

25. The method of claim 24, further comprising:

forming bit line dielectrics on said bit lines and said ONO structures; and

removing said thin oxide layer from the top surface of said oxide-conductive-layer columns.

26. The method of claim 25, further comprising depositing a second conductive layer on said substrate.

27. The method of claim 26, further comprising concurrently etching said first and second conductive layers to form word lines perpendicular to and on said bit line dielectrics and said oxide-conductive-layer columns.

28. The semiconductor structure prepared by the method of claim 5.

29. The semiconductor structure prepared by the method of claim 6.

30. The semiconductor structure prepared by the method of claim 14.

31. The semiconductor structure prepared by the method of claim 20.

32. The semiconductor structure prepared by the method of claim 24.